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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,916	01/25/2006	Tammy Cheng	DC5157 PCT1	9371

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EXAMINER

SMOOT, STEPHEN W

ART UNIT	PAPER NUMBER
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2813

NOTIFICATION DATE	DELIVERY MODE
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05/26/2009

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents.admin@dowcorning.com

Office Action Summary	Application No. 10/565,916	Applicant(s) CHENG ET AL.	
	Examiner Stephen W. Smoot	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 January 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4 and 6-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4 and 6-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 January 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>1-25-06</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office action is in response to applicant's amendment filed on 05 January 2009.

Election/Restrictions

1. Applicant's election with traverse of Group II, claims 7-16 in the reply filed on 05 January 2009 is acknowledged. However, it is noted that the applicants have also amended claim 1 to include all of the limitations of claim 7. Accordingly, the restriction requirement mailed to the applicant on 18 June 2008 is hereby withdrawn, and claims 1-2, 4, 6-16 will be examined on the merits.

In view of the withdrawal of the restriction requirement, applicants are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Specification

2. The disclosure is objected to because of the following informalities:

In the cross-reference section (see preliminary amendment filed on 25 January 2006, page 2), change both appearances of "PCT/US2004/02505" to --
PCT/US2004/025050-- to correct the application number.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Hirano et al. (US 2002/0153618 A1).

Referring to Figs. 1-10 and paragraphs [0051] to [0071], Hirano et al. disclose a semiconductor device that includes a semiconductor chip (7A) mounted onto a surface of a substrate (1) using an adhesive (9), bond wires (10) to electrically connect the chip

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(7A) to the substrate (1), a silicone-containing overmold (11) to seal the chip (7A) (see paragraph [0065]), and solder balls (12) on an opposite surface of the substrate (1).

These are all of the structural limitations as set forth in claim 6 of the applicant's invention. The remaining limitations in claim 1 are process limitations that do not impart additional structure to the electronic component as claimed in claim 6. Accordingly, per MPEP section 2113, the burden is shifted to the applicant to show an unobvious difference between the prior art of Hirano et al. and their electronic component as claimed in claim 6.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 7-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano et al. (US 2002/0153618 A1) in view of Bottini (US 3,808,673).

Referring to Figs. 1-10 and paragraphs [0051] to [0071], Hirano et al. disclose a semiconductor device that includes a semiconductor chip (7A) mounted onto a surface of a substrate (1) using an adhesive (9), bond wires (10) to electrically connect the chip (7A) to the substrate (1), a silicone-containing overmold resin (11) to seal the chip (7A)

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(see paragraph [0065]), and solder balls (12) on an opposite surface of the substrate (1). Referring to Figs. 11-13 and paragraphs [0072] to [0079], Hirano et al. further disclose that the semiconductor device can be formed by using adhesive (9) to mount the chip (7A) to a plastic film (20), connecting bond wires between the chip (7A) and the plastic film (20), placing this assembly in a mold (30) to apply the silicone-containing overmold resin (11) by injection molding, applying solder balls (12) to the opposite surface, and cutting the plastic film into a substrate (1). These are limitations as set forth in claims 7-8, 15-16 of the applicant's invention.

However, Hirano et al. lack specific details regarding their injection molding process including the clamping force between 1 to 80 tons (a limitation of claims 7, 15-16) or, more specifically, between 1 to 27 tons (the limitation of claim 9), an injection pressure between 0.3 to 7 MPa (a limitation of claims 7, 15-16), heating the mold cavity (a limitation of claims 7, 15-16), and curing the die attach adhesive (a limitation of claim 15).

Bottini teaches that a semiconductor device can be packaged by injection molding a silicone resin by curing for 120 to 150 seconds at a mold temperature of 190 degrees C, a pressure of 600 psig (i.e about 4 MPa), and a clamping force of 15 tons (see column 4, lines 25-43).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Hirano et al. and Bottini in order to use the injection molding parameters, as taught by Bottini, for sealing the

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package of Hirano et al., because Bottini shows that these are known parameters for injection molding silicon resin.

Regarding claim 10, Hirano et al. do not expressly teach or suggest that the cured silicone-containing resin is optically clear. Bottini teaches that a clear silicone resin can be used to optically couple a light emitting diode to a detector (see column 3, line 66 to column 4, line 24). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Hirano et al. by using an optically clear silicone resin, as taught by Bottini, in order to transmit light into or out of the sealed package disclosed by Hirano et al.

Regarding claims 11-12, the combination of Hirano et al. and Bottini lacks the specific mold temperature range as set forth in claim 11 or the injection pressure range as set forth in claim 12. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Hirano et al. and Bottini in order to use a mold temperature within the range of claim 11 and/or an injection pressure within the range of claim 12 through routine experimentation to discover the workable ranges of the combination [see *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)].

Regarding claims 13-14, the viscosity of the silicone composition (claim 13) and the modulus of the cured silicone composition (claim 14) are property limitations that are presumed to be inherent to the combination of Hirano et al. and Bottini, per MPEP section 2112.01, because the process for producing the silicone-containing resin of this combination is substantially identical to applicant's claim 10.

7. Claims 1, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano et al. (US 2002/0153618 A1) in view of Bottini (US 3,808,673) and Chaudhury et al. (US 2003/0145940 A1).

Referring to Figs. 1-10 and paragraphs [0051] to [0071], Hirano et al. disclose a semiconductor device that includes a semiconductor chip (7A) mounted onto a surface of a substrate (1) using an adhesive (9), bond wires (10) to electrically connect the chip (7A) to the substrate (1), a silicone-containing overmold resin (11) to seal the chip (7A) (see paragraph [0065]), and solder balls (12) on an opposite surface of the substrate (1). Referring to Figs. 11-13 and paragraphs [0072] to [0079], Hirano et al. further disclose that the semiconductor device can be formed by using adhesive (9) to mount the chip (7A) to a plastic film (20), connecting bond wires between the chip (7A) and the plastic film (20), placing this assembly in a mold (30) to apply the silicone-containing overmold resin (11) by injection molding, applying solder balls (12) to the opposite surface, and cutting the plastic film into a substrate (1). These are limitations as set forth in claims 1, 4 of the applicant's invention.

However, Hirano et al. lack specific details regarding their injection molding process including the clamping force between 1 to 80 tons (a limitation of claim 1), an injection pressure between 0.3 to 7 MPa (a limitation of claim 1), heating the mold cavity (a limitation of claim 1), and curing the die attach adhesive (a limitation of claim 1). Further, Hirano et al. lack the limitations of plasma treating a surface of the die attach adhesive, plasma treating a surface of the semiconductor die, and contacting these

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plasma treated surfaces with each other, which are also limitations as set forth in claim 1 of the applicant's invention.

Bottini teaches that a semiconductor device can be packaged by injection molding a silicone resin by curing for 120 to 150 seconds at a mold temperature of 190 degrees C, a pressure of 600 psig (i.e about 4 MPa), and a clamping force of 15 tons (see column 4, lines 25-43). Chaudhury et al. teach that surfaces of an adhesive and a semiconductor can be plasma treated in order to improve adhesion between the surfaces (see paragraphs [0017] to [0034]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Hirano et al. and Bottini in order to use the injection molding parameters, as taught by Bottini, for sealing the package of Hirano et al., because Bottini shows that these are known parameters for injection molding silicon resin. It also would have been obvious to further combine the teachings of Hirano et al. and Bottini with those of Chaudhury et al. in order to plasma treat the adhesive surface and chip surface for improved adherence.

Regarding claim 4, the viscosity range for the silicone composition (a limitation of claim 4) and the modulus range for the cured silicone composition (a limitation of claim 4) are property limitations that are presumed to be inherent to the combination of Hirano et al., Bottini, and Chaudhury et al., per MPEP section 2112.01, because the process for producing the silicone-containing resin of this combination is substantially identical to applicant's claim 1.

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8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano et al. (US 2002/0153618 A1), Bottini (US 3,808,673), and Chaudhury et al. (US 2003/0145940 A1) as applied to claim 1 above, and further in view of Takeuchi et al. (US 6,475,629 B1).

As shown above, the combination of Hirano et al., Bottini, and Chaudhury et al. has all of the limitations as set forth in claim 1 of the applicant's invention. However, this combination does not expressly teach or suggest that the die attach adhesive includes silicone, which is the further limitation to claim 1 as set forth in claim 2 of the applicant's invention. Takeuchi et al. teach that a die attach adhesive (4) can include a siloxane-based resin (see Fig. 5 and column 14, line 54 to column 15, line 6).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Hirano et al., Bottini, Chaudhury et al., and Takeuchi et al. in order to include silicone material in the die attach adhesive like the siloxane resin of Takeuchi et al., because Takeuchi et al. recognize that the siloxane resin exhibits strong adhesion (see column 25, lines 46-54).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on Monday to Friday from 8:00am to 4:30pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Landau can be reached on 571-272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen W Smoot/
Primary Examiner
Art Unit 2813

SWS